Remarks

Applicants respectfully request reconsideration of this application as amended. Claims 1, 3, 4, 7, 11, 13, 14, 16, 17, and 20-22 have been amended. Claims 9, 10, and 12 have been cancelled. Claims 23-25 have been added. Therefore, claims 1-8, 11, and 13-25 are presented for examination.

35 U.S.C. §103(a) Rejection

Claims 1-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Hirairi (U.S. Patent No. 6,480,942) and further in view of "Data Structures with C++" by William Ford and William Topp (hereinafter "Ford & Topp"). Applicants submit that the present claims are patentable over any combination of Hirairi and Ford & Topp.

Hirairi discloses a synchronized FIFO memory circuit including random access memory and a FIFO controller. (Hirairi at Abstract.) The FIFO circuit of Hirairi is designed to reduce the length of the critical path in the FIFO controller by raising the operating speed of the FIFO controller itself. (Col. 4, lines 25-28.) The FIFO controller circuitry includes elements to produce status signals of the FIFO memory circuit, namely, Write Ready, Read Ready, Full, Empty, Almost Full and Almost Empty at a high speed. (Col. 4, lines 32-42.)

Ford & Topp discloses basic background information about queues as applied in computer programming. More specifically, specific operations on queues in the programming language C++ are discussed. (Ford & Topp at pages 204-208.)

Claim 1, as amended, recites:

> An apparatus, comprising:
> a queue;
> a programmable event conditioning logic unit to receive a queue enter signal, a queue exit signal, and a queue not

empty signal from the queue, the queue enter signal to be asserted in response to an entry entering the queue, the queue exit signal to be asserted in response to an entry exiting the queue, and the queue not empty signal to indicate that the queue contains at least one entry; and

a first counter to increment in response to a first increment event signal delivered by the event selection logic unit, the first counter to decrement in response to a first decrement event signal delivered by the event selection logic unit;

a second counter to increment in response to a second increment event signal delivered by the event selection logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event selection logic unit,

wherein assertion of at least one of the second increment event signal and the second decrement event signal is based on a value of the first counter.

Applicants submit Hirairi does not disclose or suggest a second counter to increment in response to a second increment event signal delivered by the event selection logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event selection logic unit, wherein assertion of at least one of the second increment event signal and the second decrement event signal is based on a value of the first counter. Applicants can find no disclosure or suggestion of such a feature in Hirairi. Furthermore, Ford & Topp does not disclose or suggest a second counter to increment in response to a second increment event signal delivered by the event selection logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event selection logic unit, wherein assertion of at least one of the second increment event signal and the second decrement event signal is based on a value of the first counter.

Since neither Hirairi nor Ford & Topp disclose or suggest such a feature, any combination of Hirairi and Ford & Topp would also not disclose or suggest it. Therefore, claim 1 is patentable over Hirairi in view of Ford & Topp.

Claims 2-6 depend from claim 1 and include additional limitations. Therefore, claims 2-6 are also patentable over Hirairi in view of Ford & Topp.

Claim 7, as amended, recites:

> An apparatus, comprising:
> a queue;
> a programmable event conditioning logic unit to receive a queue enter signal, a queue exit signal, and a queue not empty signal from the queue, the queue enter signal to be asserted in response to an entry entering the queue, the queue exit signal to be asserted in response to an entry exiting the queue, and the queue not empty signal to indicate that the queue contains at least one entry; and
> a first counter to increment in response to a first increment event signal delivered by the event selection logic unit, the first counter to decrement in response to a first decrement event signal delivered by the event selection logic unit;
> a data register coupled to the first counter;
> a comparator including a first input, a second input, and an output, the first input coupled to the data register, the second input coupled to the first counter, and the output provided to the event conditioning logic unit; and
> a second counter to increment in response to a second event signal delivered by the event selection logic unit, the second event signal in response to the comparator output indicating that the first counter value matches the data register value.

Applicants submit that Hirairi does not disclose or suggest a data register coupled to a first counter, a comparator, and a second counter to increment in response to a second event signal generated in response to the comparator indicating that the first counter value matches the data register value. Applicants can find no disclosure or suggestion of such a feature in Hirairi. Furthermore, applicants submit that Ford & Topp also does not disclose or suggest such a feature. Since neither Hirairi nor Ford & Topp disclose or suggest such a feature, any

combination of Hirairi and Ford & Topp would also not disclose or suggest it. Therefore, claim 7 is patentable over Hirairi in view of Ford & Topp.

Claims 8, 11, 13, and 23-25 depend from claim 7 and include additional limitations. Therefore, claims 8, 11, 13, and 23-25 are also patentable over Hirairi in view of Ford & Topp.

Claim 14, as amended, recites, in part, a second counter to increment in response to a second increment event signal delivered by the event selection logic unit, the second counter to decrement in response to a second decrement event signal delivered by the event selection logic unit, wherein assertion of at least one of the second increment event signal and the second decrement event signal is based on a value of the first counter. Similar to the discussion above, neither Hirairi nor Ford & Topp disclose or suggest such a feature. As a result, claim 14 is patentable over Hirairi in view of Ford & Topp for the reasons discussed above with respect to claim 1. As claims 15-19 depend from claim 14 and include additional limitations, claims 15-19 are also patentable over Hirairi in view of Ford & Topp.

Claim 20, as amended, recites, in part, asserting a second event signal and incrementing a second counter in response to the assertion of the second event signal, the second event signal asserted in response to the first counter matching a threshold value. Similar to the discussion above, neither Hirairi nor Ford & Topp disclose or suggest such a feature. As a result, claim 20 is patentable over Hirairi in view of Ford & Topp for the reasons discussed above with respect to claim 1. As claims 21 and 22 depend from claim 20 and include additional limitations, claims 21 and 22 are also patentable over Hirairi in view of Ford & Topp.

Applicants respectfully submit that the rejections have been overcome and that the claims are in condition for allowance. Accordingly, applicants respectfully request the rejections be withdrawn and the claims be allowed.

The Examiner is requested to call the undersigned at (303) 740-1980 if there remains any issue with allowance of the case.

Applicants respectfully petition for an extension of time to respond to the outstanding Office Action pursuant to 37 C.F.R. § 1.136(a) should one be necessary. Please charge our Deposit Account No. 02-2666 to cover the necessary fee under 37 C.F.R. § 1.17(a) for such an extension.

Please charge any shortage to our Deposit Account No. 02-2666.

Respectfully submitted,

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